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Model Name : AIZY0  
File Name : LA-B921PR10  
BOM P/N:43xxxxxxxx

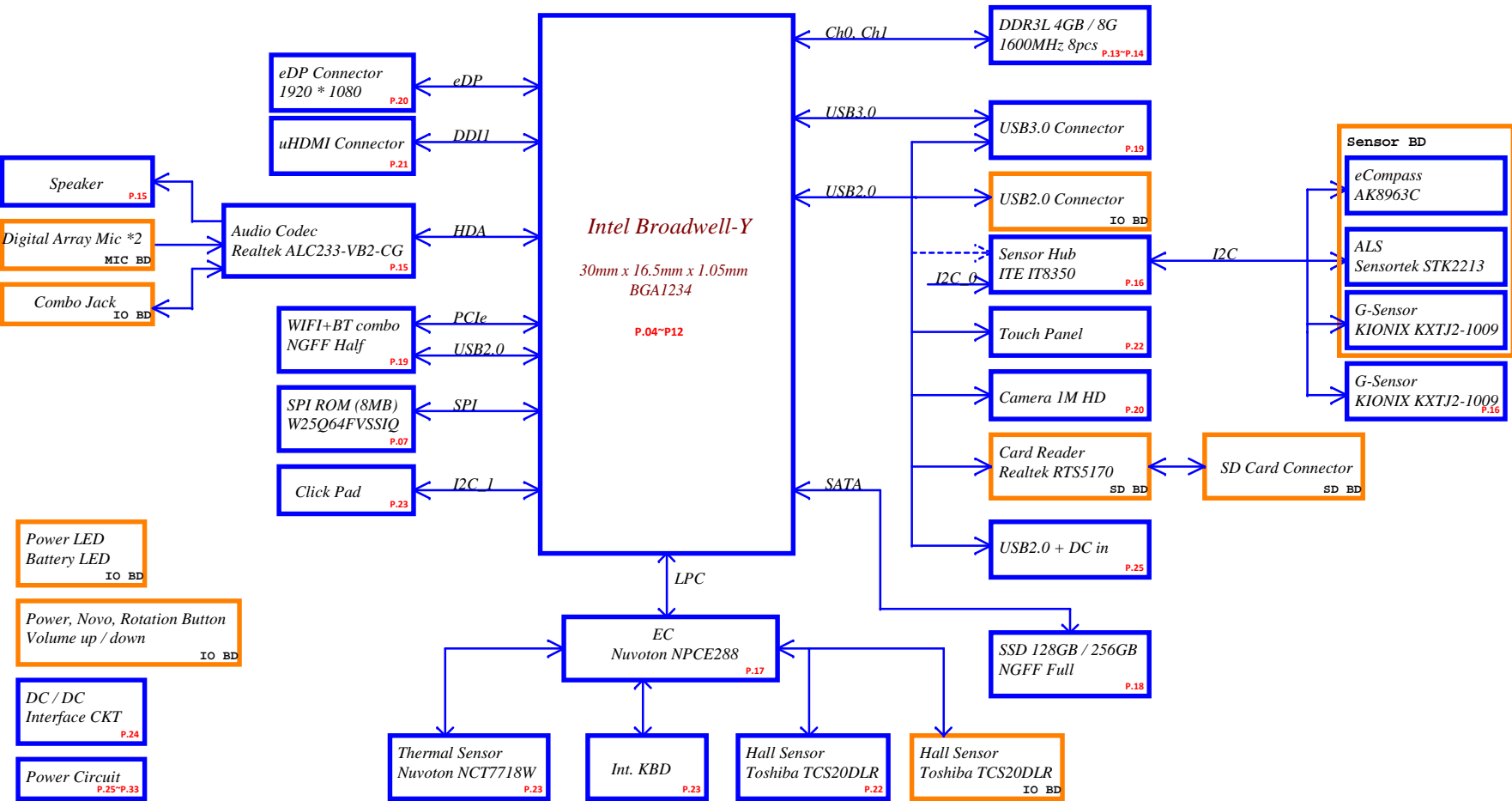
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AIZY0 M/B Schematics Document  
Intel Broadwell Y Processor

2014-09-30  
REV:1.0

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AIZY0 Intel Broadwell Y Block Diagram



## Voltage Rails

power plane	B+	+5VALW +3VALW	+1.35V	+5VS +3VS +1.5VS +1.05VS_VTT +CPU_CORE +0.675VS
State				
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

STATE	SIGNAL	SLP_S0#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

## BOM Structure Table

BTO Item	BOM Structure
Connector	ME@
76 LEVEL	X76@
UNPOP	@
CPU OPTION	CPU1@ ~ CPU8@
DRAM Option	H4G@ E4G@ S4G@ M4G1@ S8G@ E8G@ H8G@ M8G@ M4G2@
EMI POP	EMI@
ESD POP	ESD@
EMI UNPOP	@EMI@
ESD UNPOP	@ESD@
WLAN Support ISCT	ISCT@
WLAN No Support ISCT	NoISCT@

## EC SM Bus1 address

Device	Address
Smart Battery	
Charger	
Home Key Button(TS)	8bit:0x60, 7bit:0x30

## EC SM Bus2 address

Device	Address
Thermal Sensor NCT7718W	1001100x
Broadwell ULT SML1	

## CPU SM Bus address

Device	Address
NA	

## CPU SML0 Bus address

Device	Address
NA	

## USB 2.0 Port Table

USB 2.0 Port	3 External USB Port
0	USB 2.0 Port (I/O Board)
1	USB 3.0/2.0 Port (MB)
2	DCIN USB COMBO
3	Card Reader
4	Touch Screen
5	Camera
6	Mini Card (WLAN/BT)
7	Sensor Fusion

## USB 3.0 Port Table

Port	
1	
2	USB 3.0 Port (MB)
3	
4	

## PCIe Port Table

Port	Lane	
1		
2		
3		
4		NGFF WLAN
5	0	
	1	
	2	
	3	
6	0	
	1	
	2	
	3	

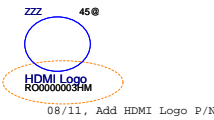
## SATA Port Table

Port	
3	
2	
1	NGFF SSD(SATA)
0	

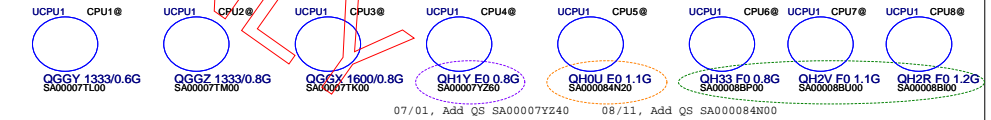
## SMBUS Control Table

	HOST	Changer	BATT	NPCE288	CPU	HomeKey	Thermal sensor NCT7718W
EC_SMB_CK1	NPCE288 +3VLP	+3VLP	+3VLP	X	X	+3VALW	X
EC_SMB_DA1	NPCE288 +3VLP	X	X	X	X	+3VALW	X
EC_SMB_CK2	NPCE288 +3VS	X	X	X	X	+3VS	X
SMBCLK	CPU +3VALW	X	X	X	X	X	X
SMBDATA	CPU +3VALW	X	X	X	X	X	X
SML0CLK	CPU +3VALW	X	X	X	X	X	X
SML0DATA	CPU +3VALW	X	X	X	X	X	X
SML1CLK	CPU +3VS	X	X	X	X	X	X
SML1DATA	CPU +3VS	X	X	X	X	X	X

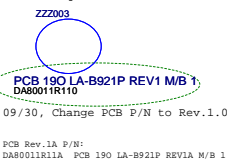
## HDMI Logo



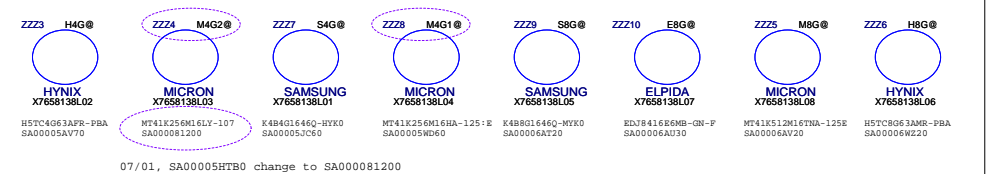
## CPU part



## PCB part



## DRAM



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## Compal Electronics, Inc.

## Note List

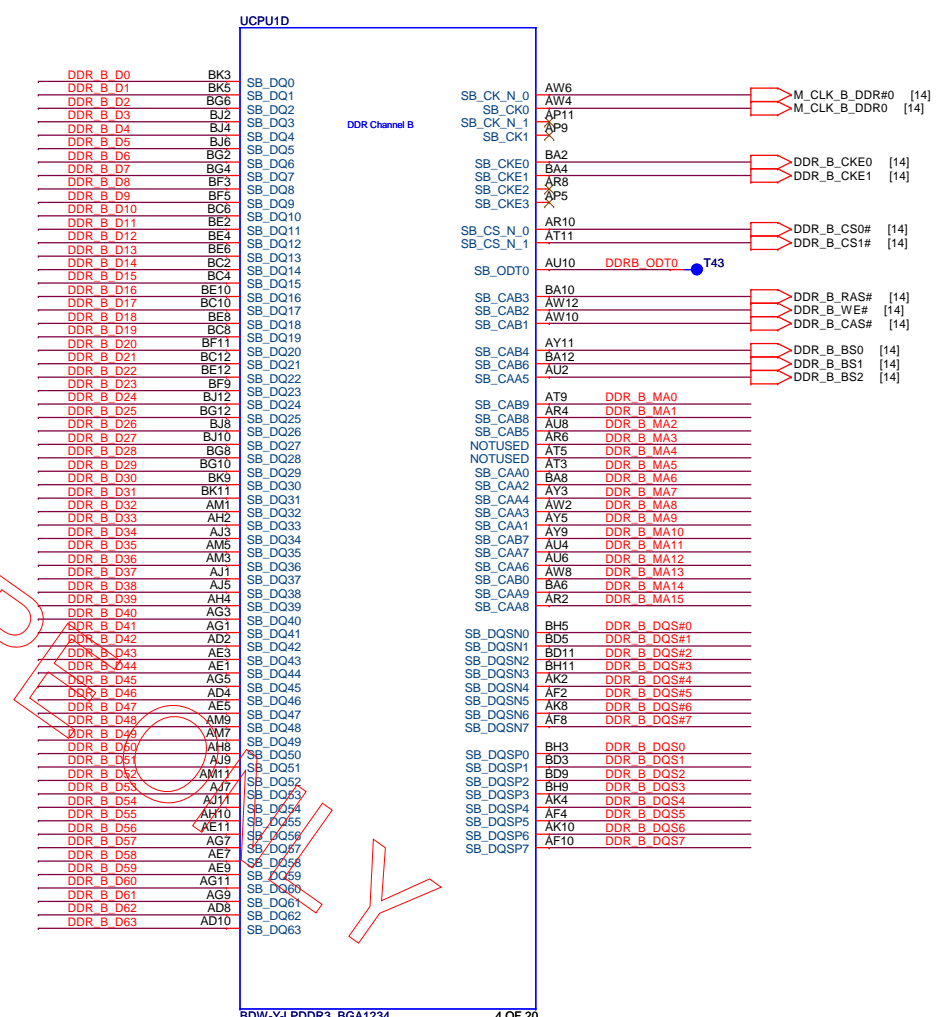
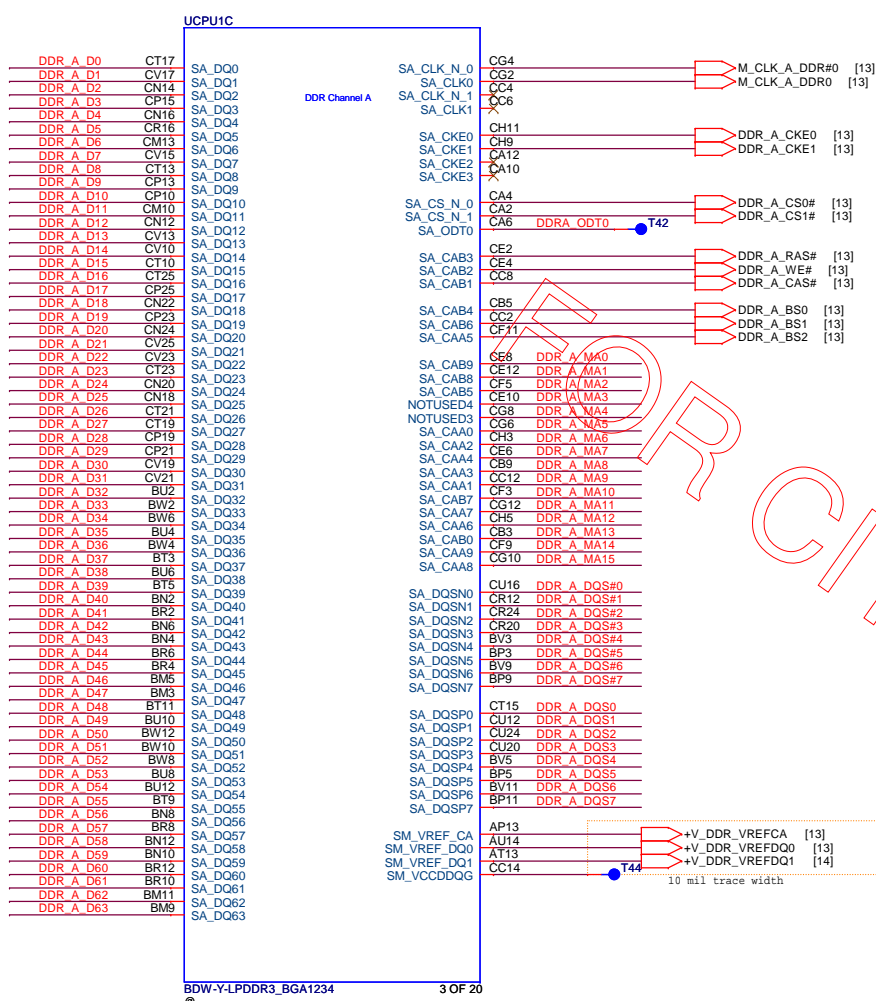
## LA-B921PR10

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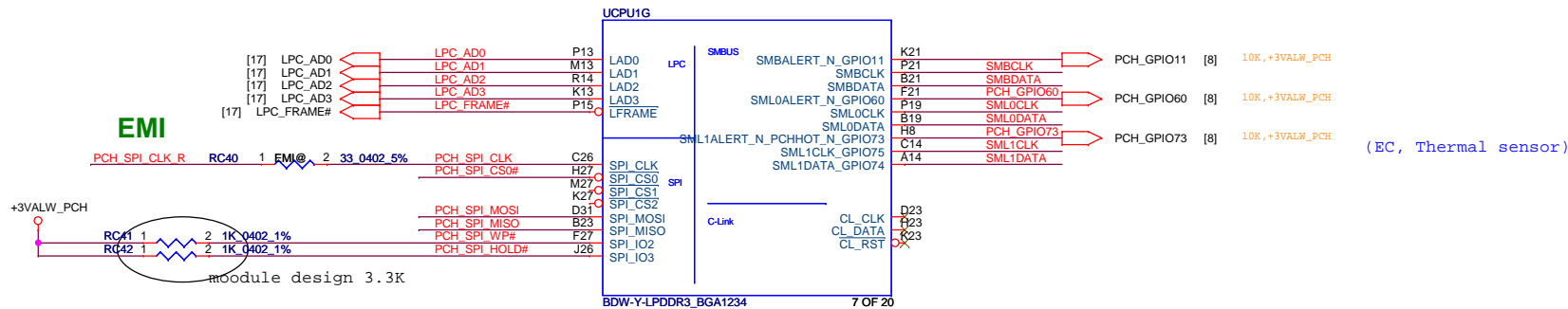


[13] DDR\_A\_D[0..63]  
[13] DDR\_A\_MA[0..15]  
[13] DDR\_A\_DQS#[0..7]  
[13] DDR\_A\_DQS[0..7]

[14] DDR\_B\_D[0..63]  
[14] DDR\_B\_MA[0..15]  
[14] DDR\_B\_DQS#[0..7]  
[14] DDR\_B\_DQS[0..7]





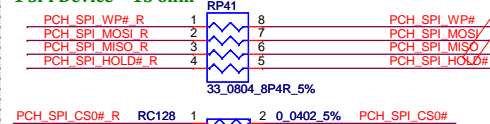


Closed to ROM

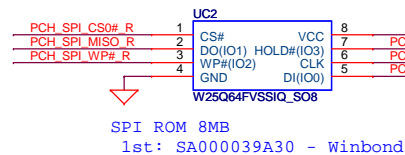
**CHKLIST1.0**

2 SPI Device = 33 ohm

1 SPI Device = 15 ohm



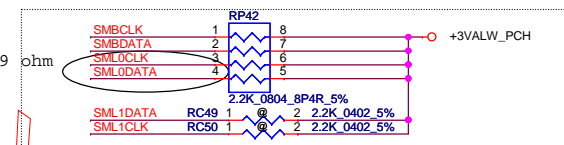
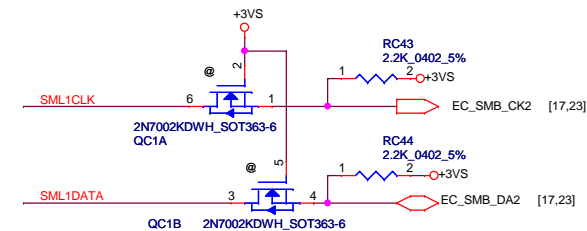
**SPI ROM FOR ME ( 8MByte )**  
**ROM is Quad SPI**



SML1 Bus BIOS set Native,  
it's OD pin

**SML1 Bus :EC/Thermal Sensor**

FootPrint :DMN6D0LDW-7\_SOT363-6



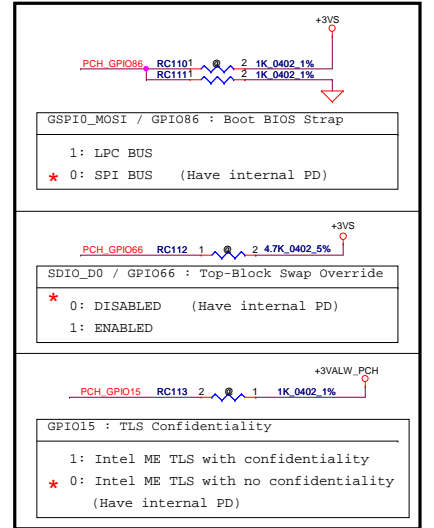
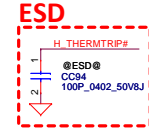
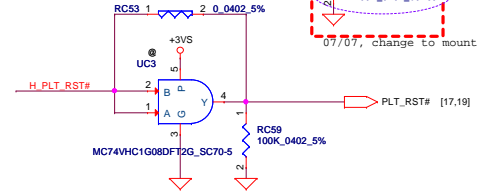
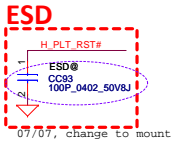
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
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2017/04/10				Title				BDW MCP(4/9) LPC,SPI,SMBUS			
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Note: SUSACK# and SUSWRN# can be tied together if EC does not want to involve in the handshake mechanism for the Deep Sleep state entry and exit CAN be NC ,if not support Deep Sx

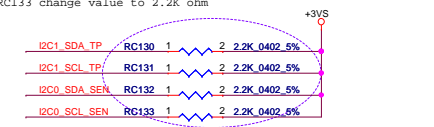
DPWROK: Tired together with RSMRST# that do not support Deep Sx

DSWODVREN - On Die DSW VR Enable  
★ H : Enable(DEFAULT)  
L : Disable

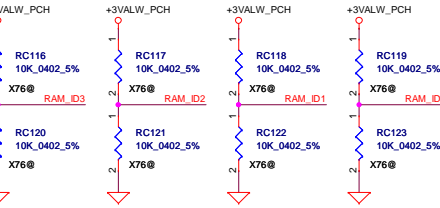
DPWROK can be tied to RSMRST# for platforms that do not support the Deep Sx state.



06/30, RC130-RC133 change value to 2.2K ohm

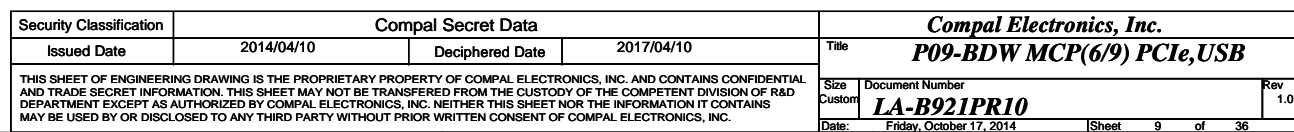


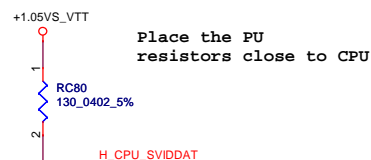
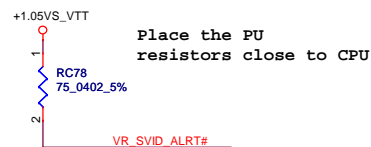
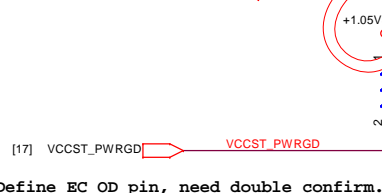
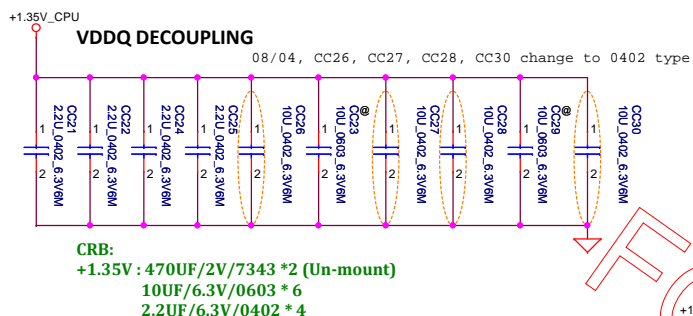
RAM_ID3	RAM_ID2	RAM_ID1	RAM_ID0	RAM P/N
GPIO59	GPIO58	GPIO57	GPIO56	
0	0	0	0	HYNIX H5TC4G63AFR-PBA
0	0	0	1	SAMSUNG K4B4G1646Q-HYK0
0	0	1	0	MICRON MT41K256M16HA-125:E
0	0	1	1	ELPIDA EDJ4216EFBG-GN-F
0	1	0	0	SAMSUNG K4B8G1646Q-MYK0
0	1	0	1	ELPIDA EDJ8416E6MB-GN-F
0	1	1	0	MICRON MT41K512M16TNA-125:E
0	1	1	1	HYNIX H5TC8G63AMR-PBA
1	0	0	0	MT41K256M16LY-107
1	0	0	1	TBD
1	0	1	0	TBD
1	0	1	1	TBD
1	1	0	0	TBD
1	1	0	1	TBD
1	1	1	0	TBD
1	1	1	1	TBD



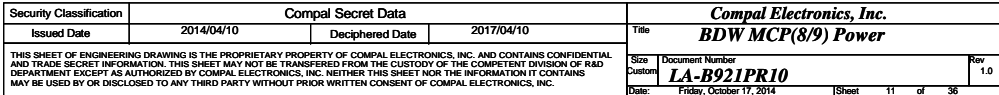
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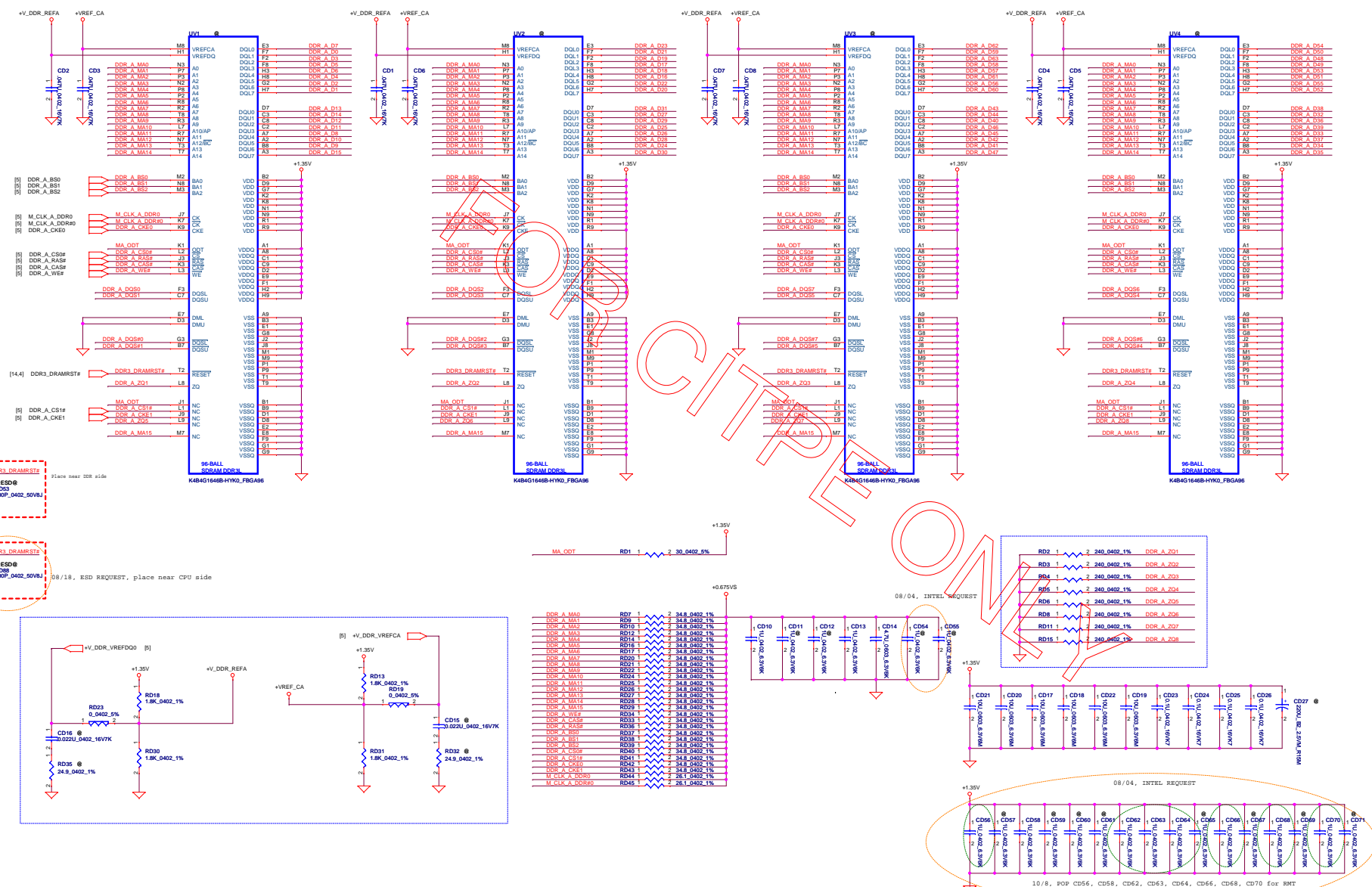


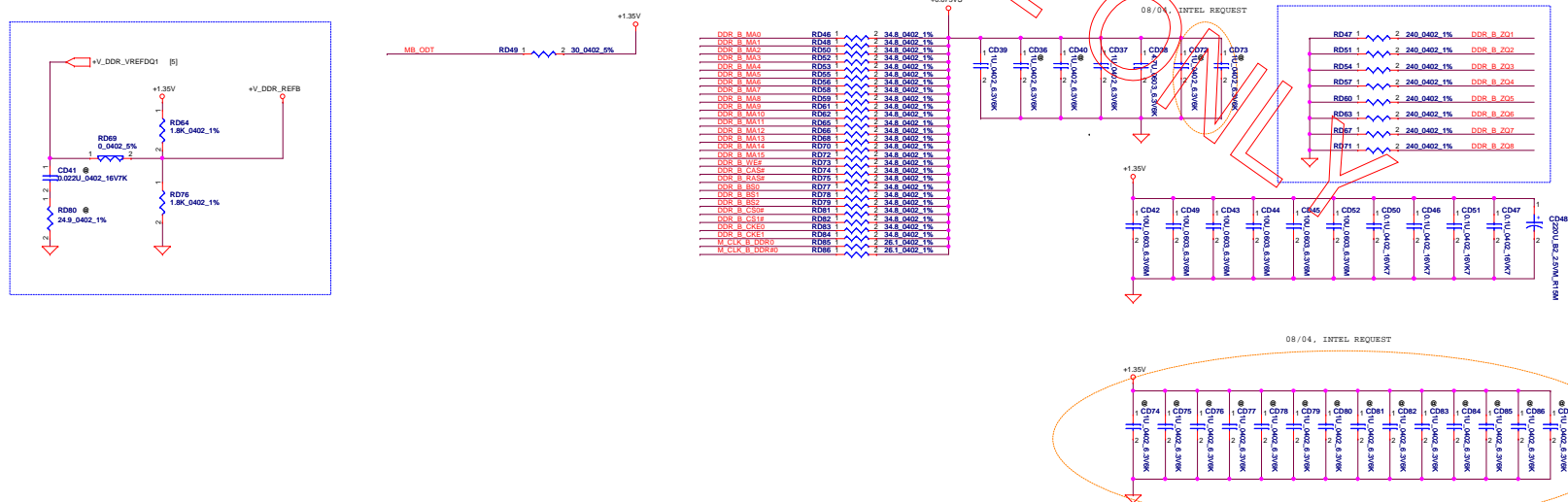
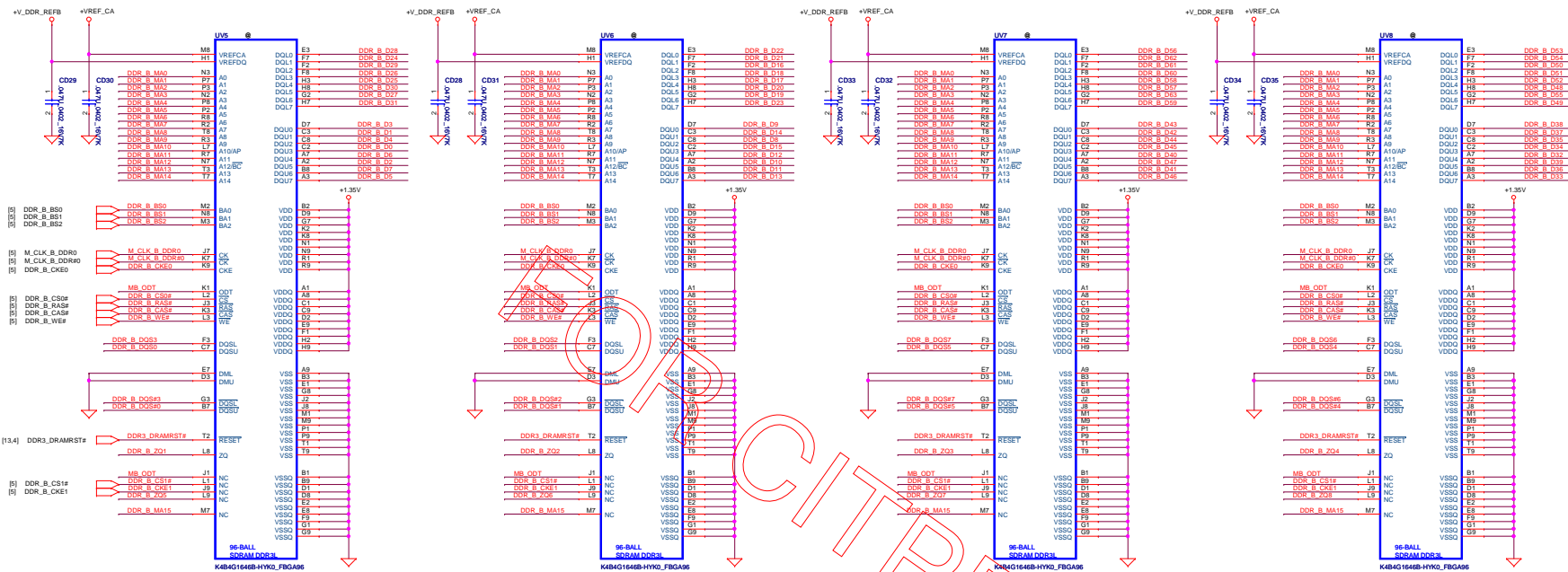
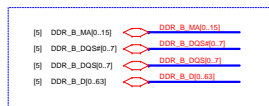


**CAD Note: PD resistor should be close to CPU**

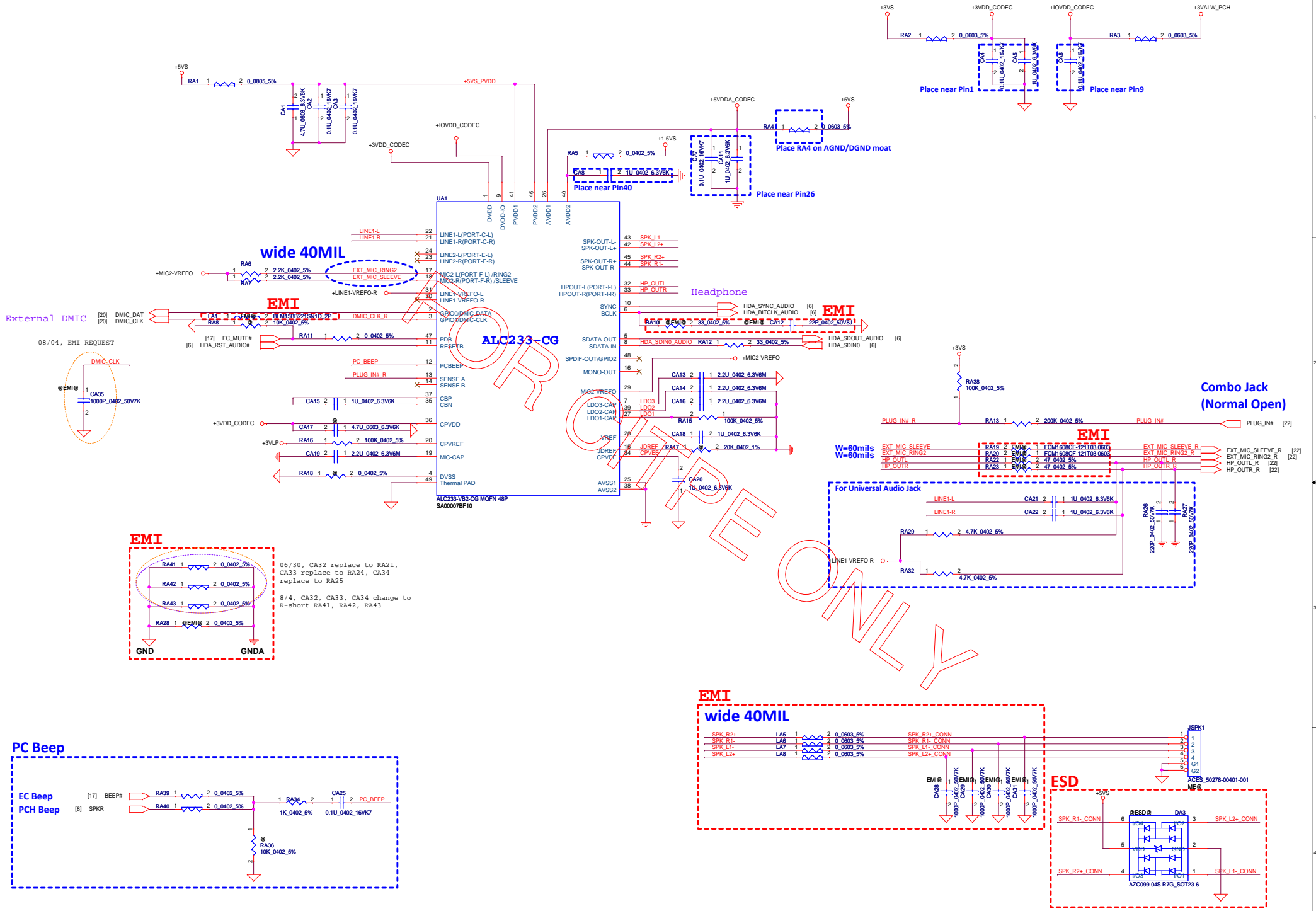






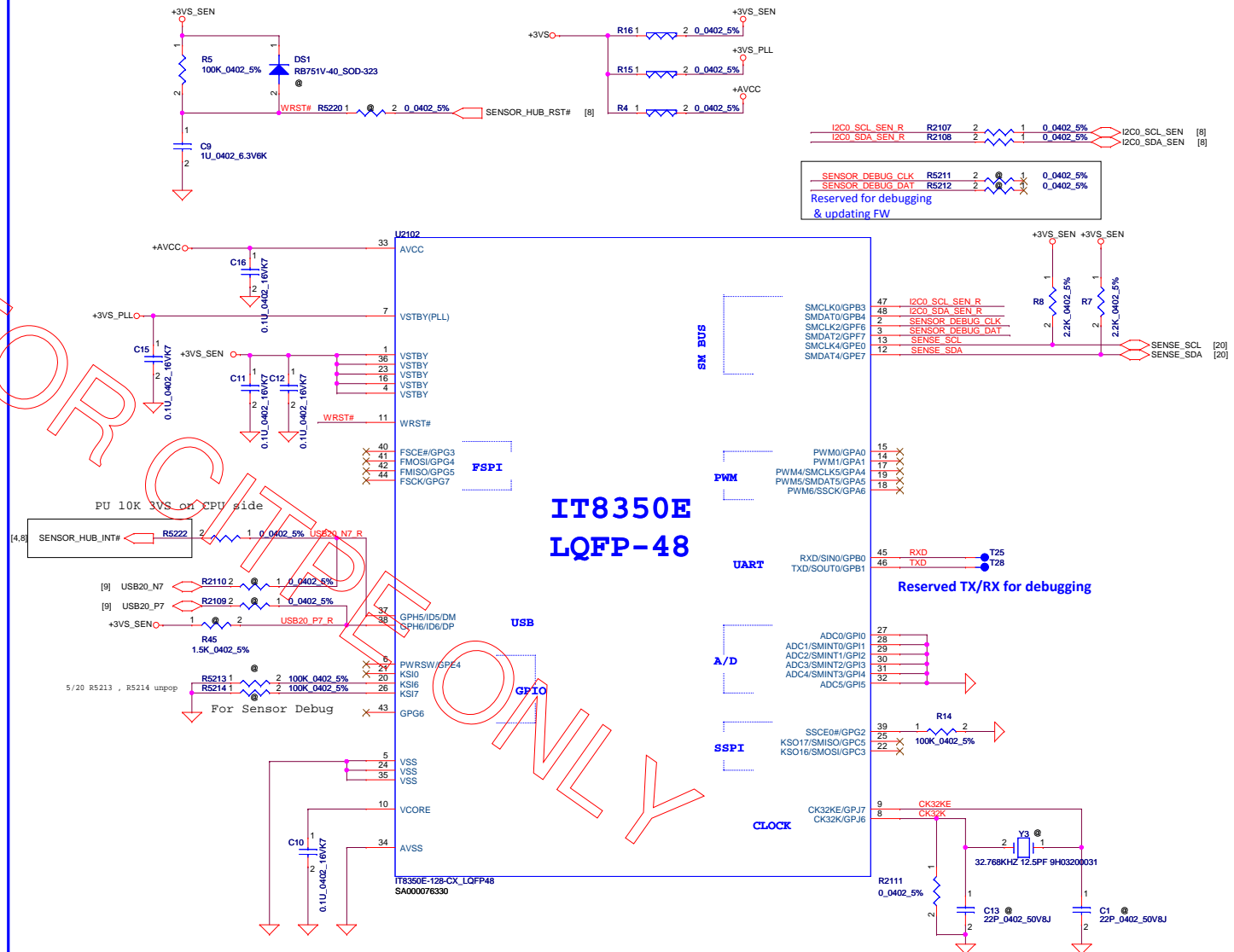
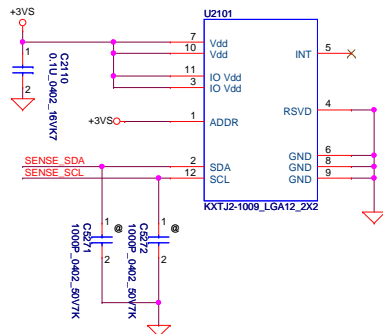


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			New Date Feb-09-2011	
			Rev 16	



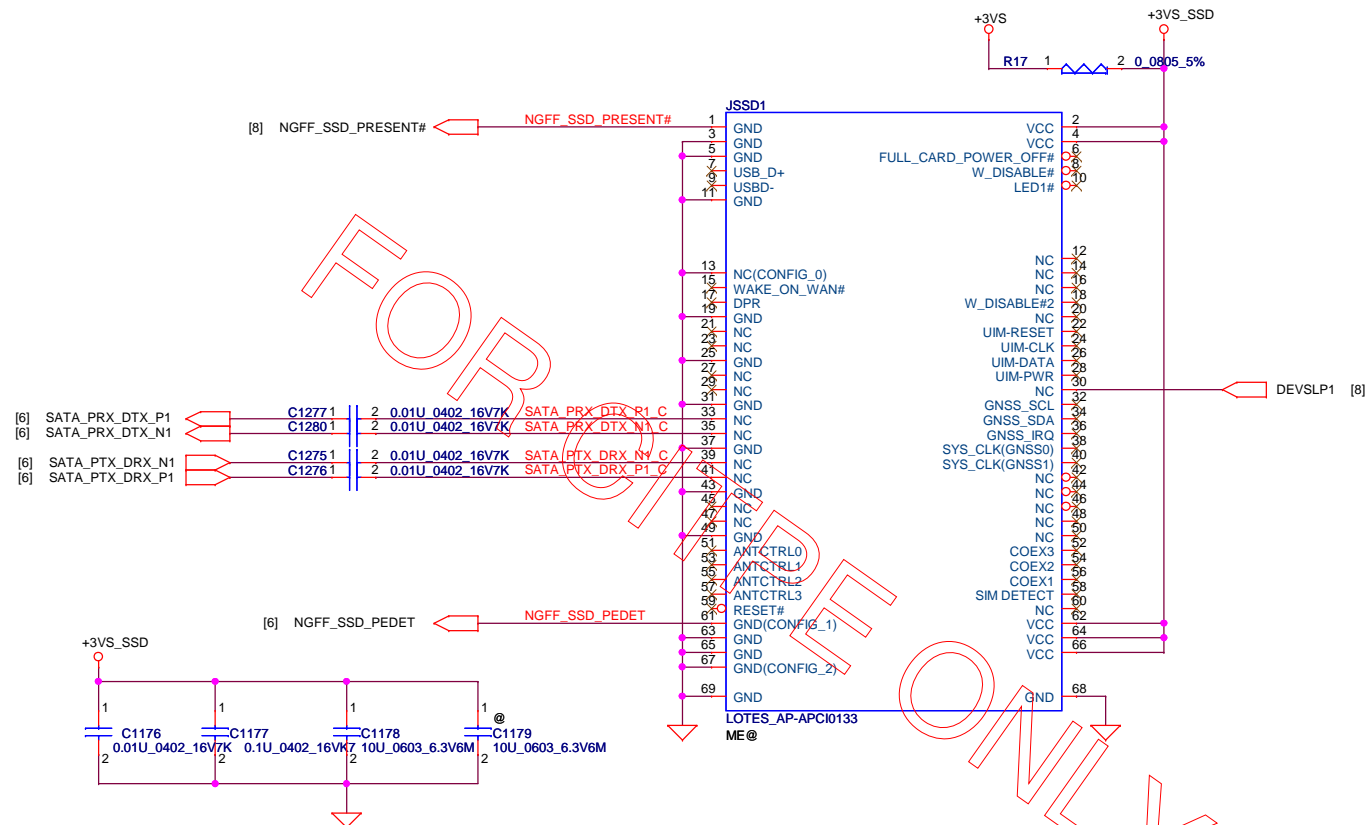
## 2nd G-sensor

## Sensor Hub



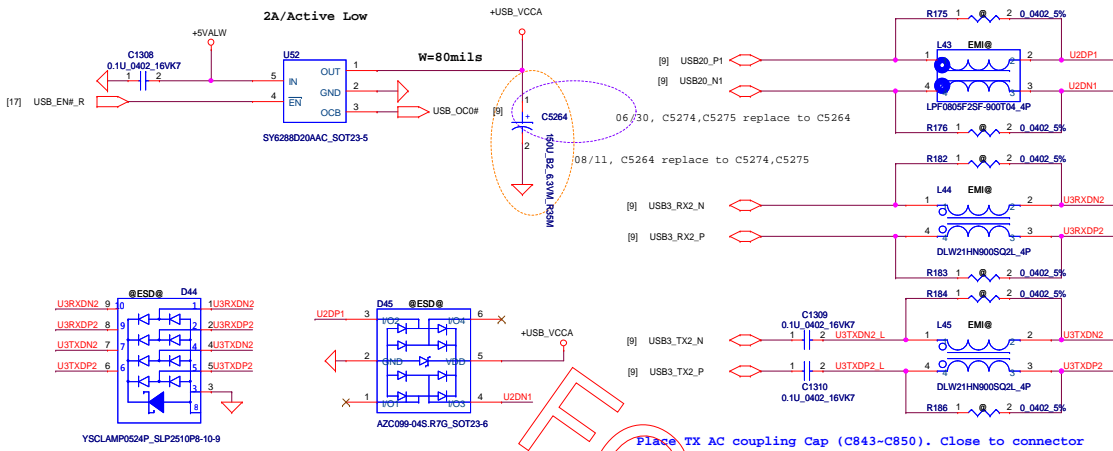


# NGFF for SSD(Key B)

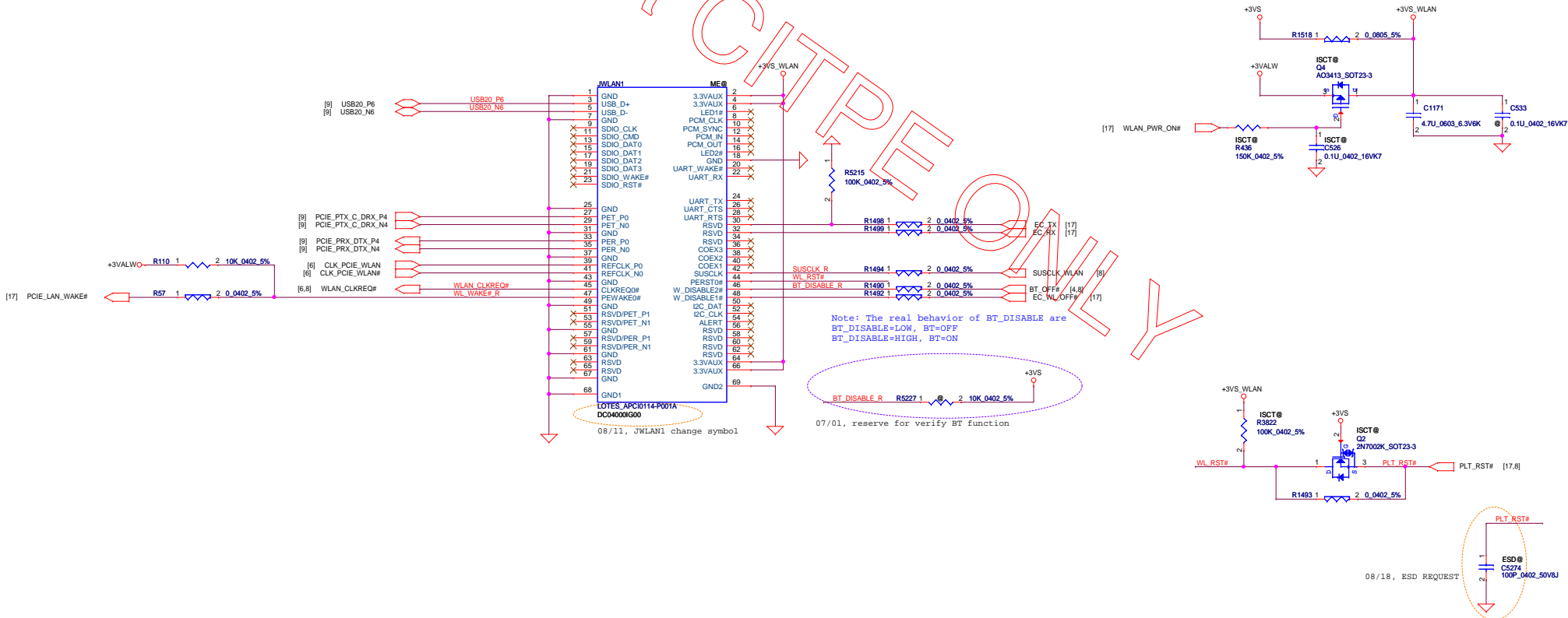


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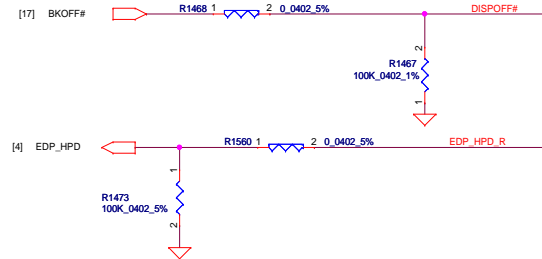
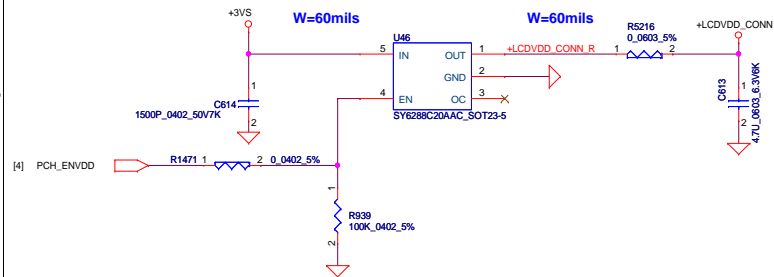
USB 3.0 Conn.



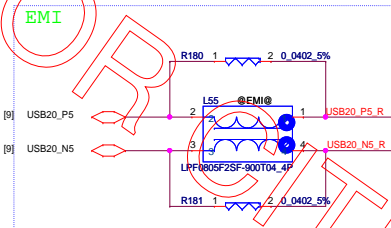
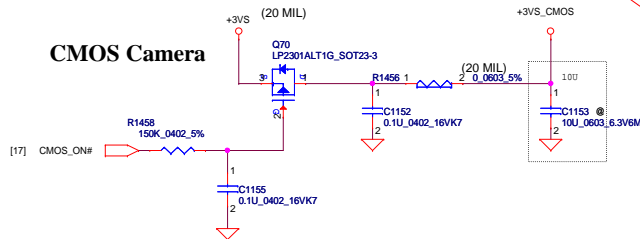
NGFF for WLAN(Key E)



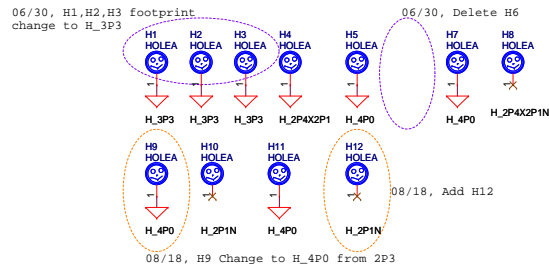
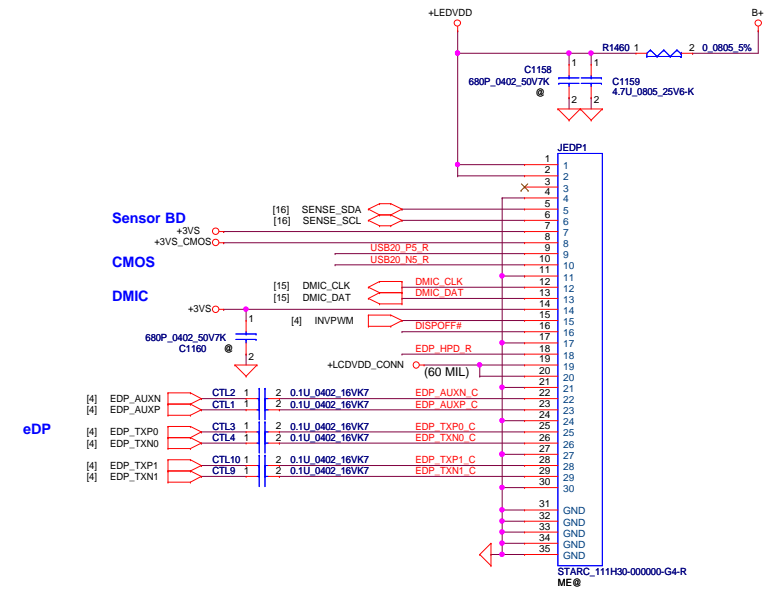
## LCD POWER CIRCUIT



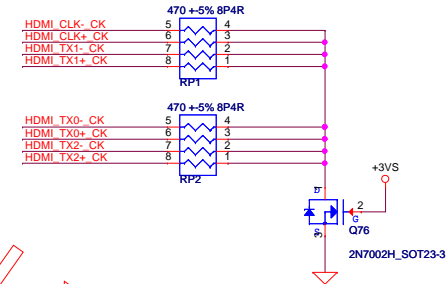
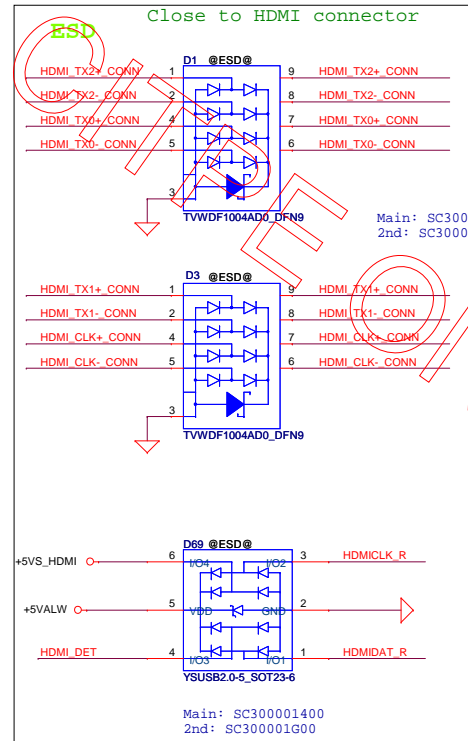
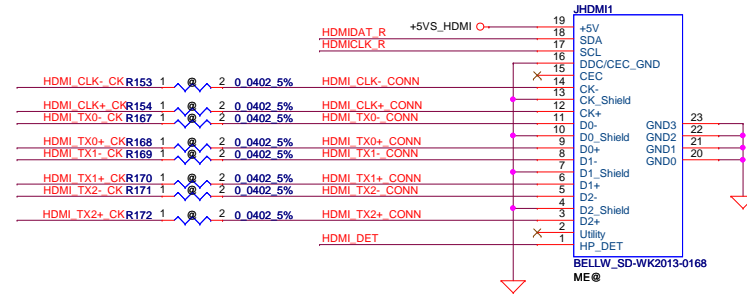
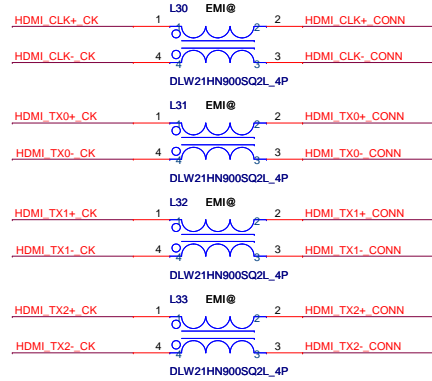
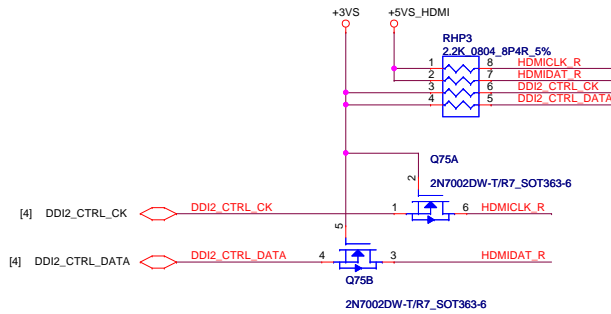
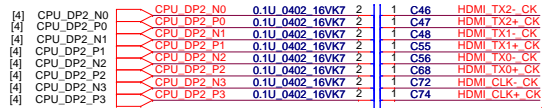
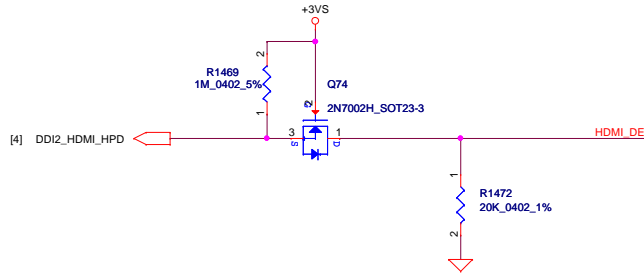
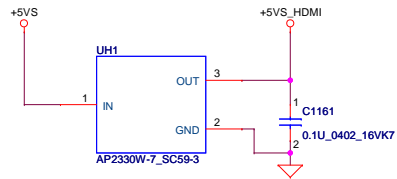
## CMOS Camera



## eDP PANEL/DMIC/COMS/SENSOR. Conn.

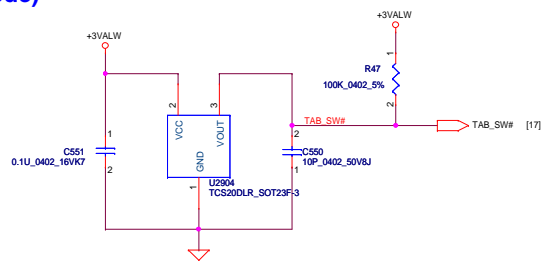


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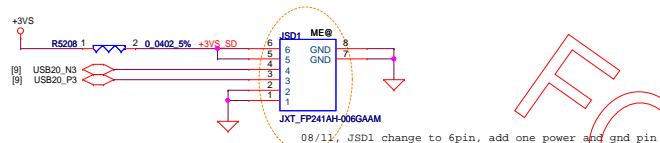


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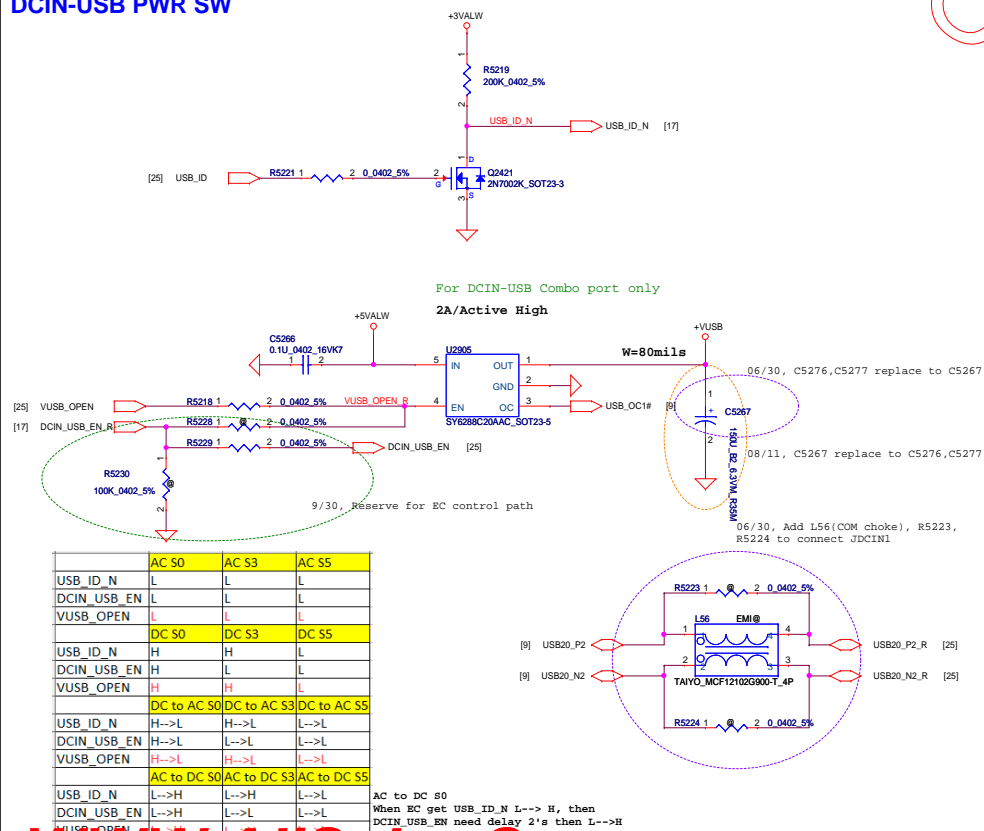
# Lid SW(Tablet Mode)



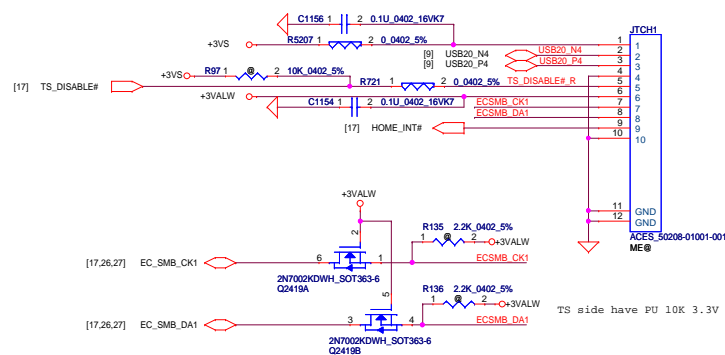
# SD Board



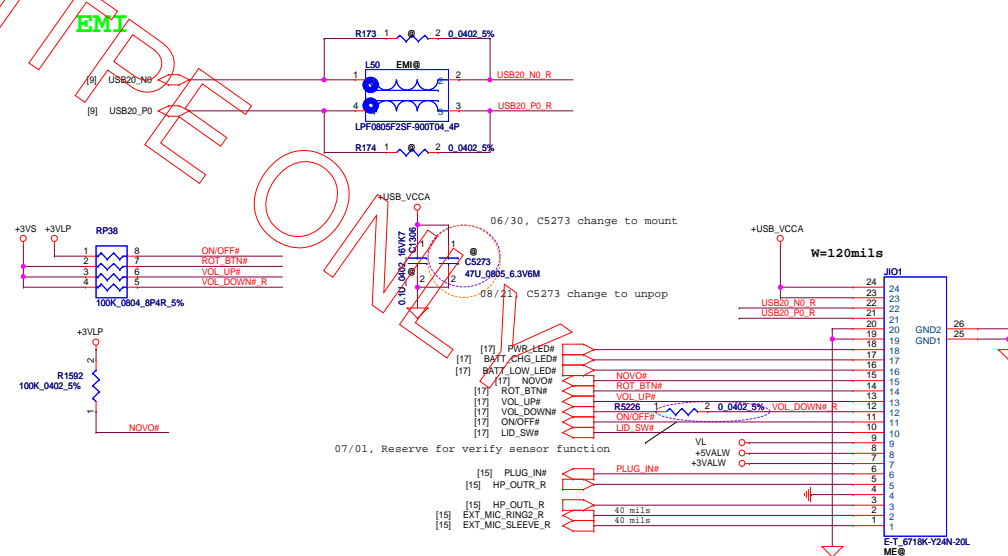
# DCIN-USB PWR SW



# Touch Panel



# I/O Board

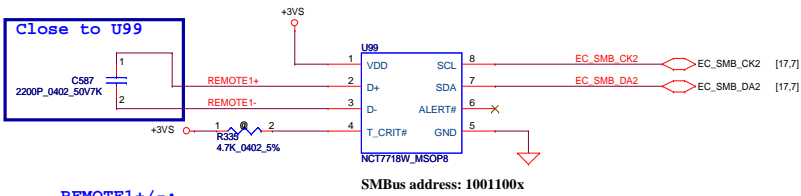


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				C	LA-B921PR10
				Date: Thursday, October 23, 2014 10:48:41 AM of 36	

Thermal Sensor

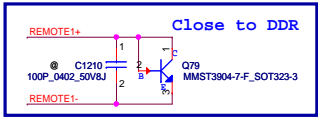
Keyboard

Close to U99

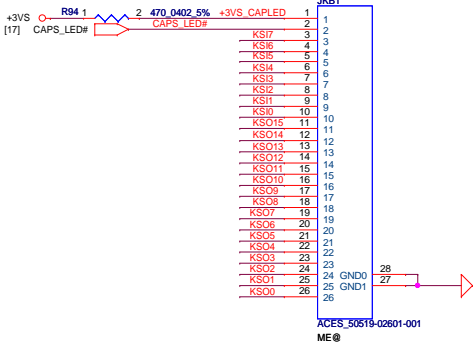
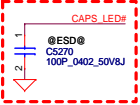


REMOTE1+/-:  
Trace width/space:10/10 mil  
Trace length:<8"

Close to DDR

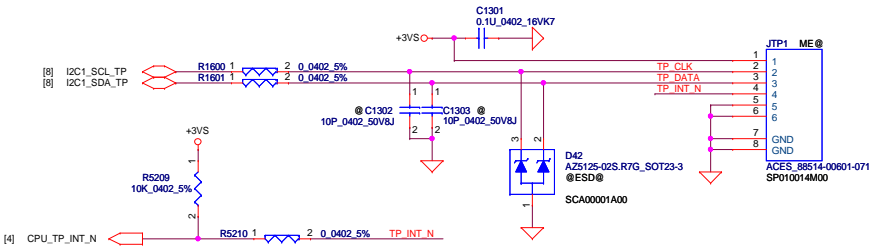


ESD



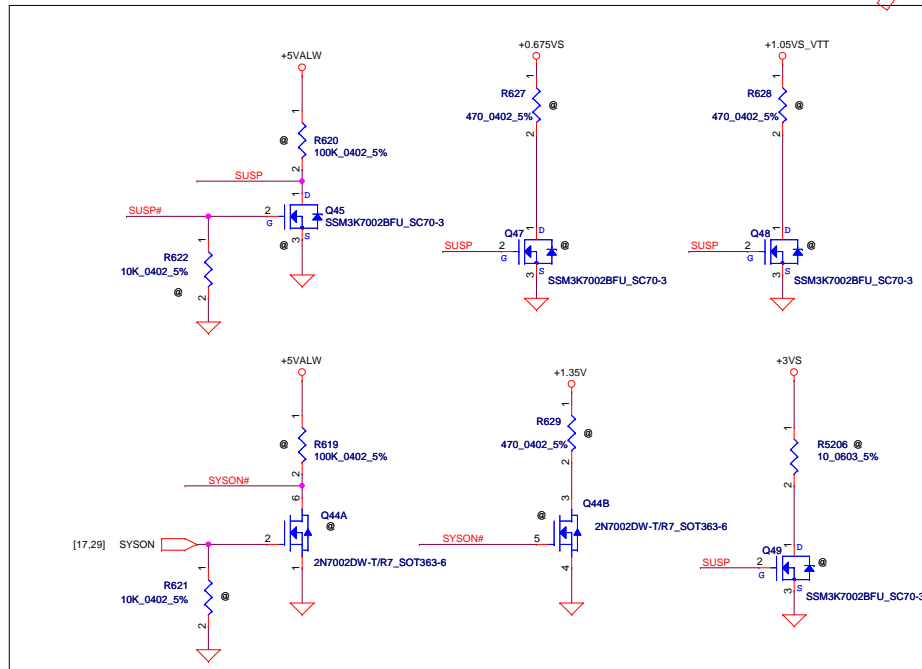
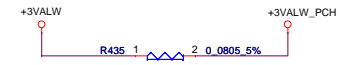
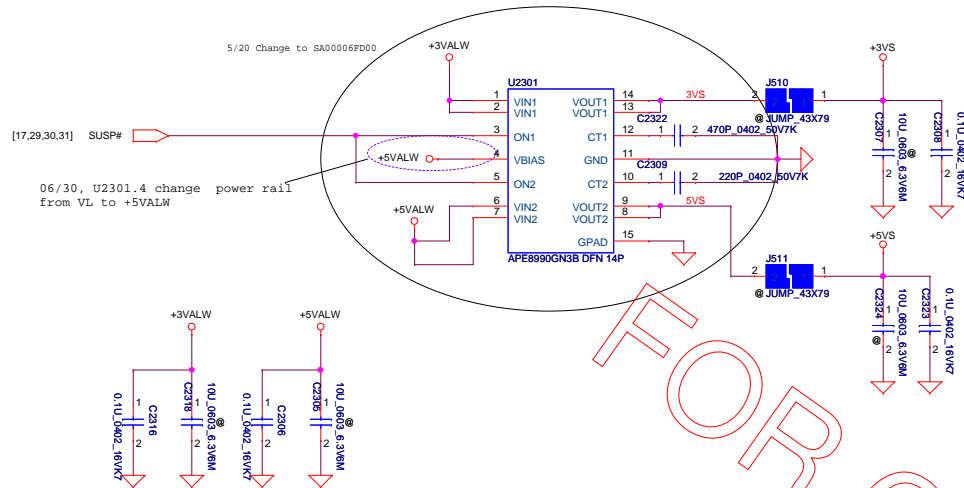
PIN1	+3VALW
PIN2	CAP_LED
PIN3	KS17
PIN4	KS16
PIN5	KS15
PIN6	KS14
PIN7	KS13
PIN8	KS12
PIN9	KS11
PIN10	KS10
PIN11	KS015
PIN12	KS014
PIN13	KS013
PIN14	KS012
PIN15	KS011
PIN16	KS010
PIN17	KS09
PIN18	KS08
PIN19	KS07
PIN20	KS06
PIN21	KS05
PIN22	KS04
PIN23	KS03
PIN24	KS02
PIN25	KS01
PIN26	KS00

Click Pad



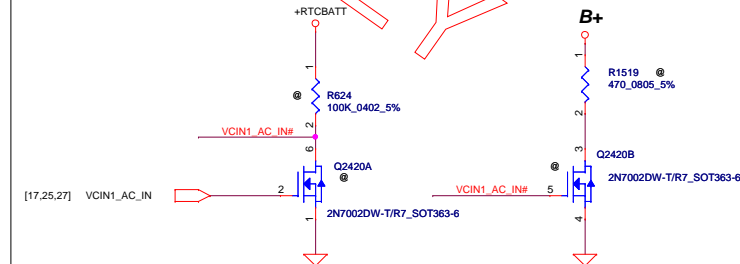
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Issued Date	2014/04/10	Deciphered Date	2017/04/10
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		Size	Document Number
		Custom	LA-B921PR10
		Date	Friday, October 17, 2014
		Sheet	23 of 36
		Rev	1.0

+5VALW TO +5VS  
+3VALW TO +3VS



Use for panel sequence

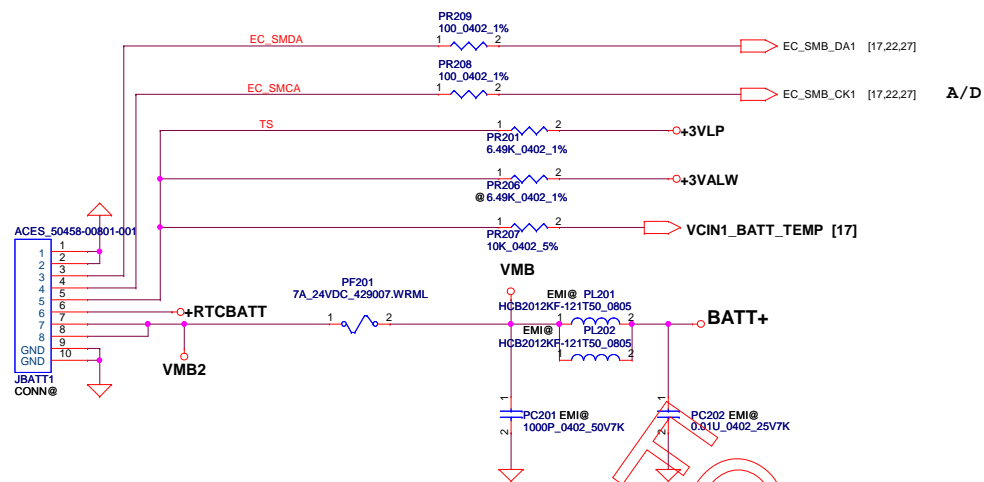
**B+ discharger**



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2014/04/10				2017/04/10				Title			
2017/04/10				DC V TO VS INTERFACE				Size			
CUSTOM				LA-B921PR10				Rev			
1.0				Date: Friday, October 17, 2014				Sheet 24 of 36			

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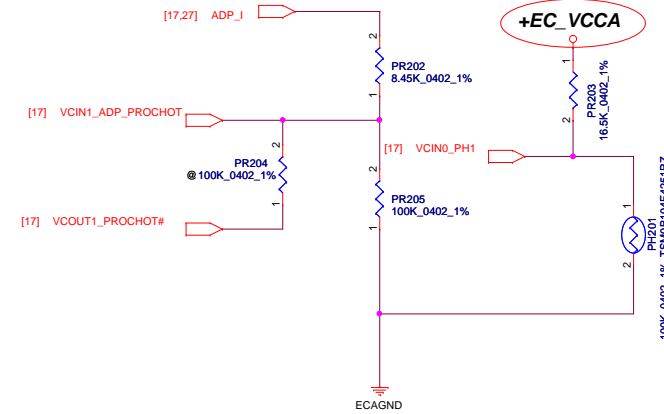




PH201 under CPU bottom side :  
CPU thermal protection at 93  $\pm$  3 degree C  
Recovery at 56  $\pm$  3 degree C

65W(UMA): 85W active W recovery

20120314  
Change to +EC\_VCCA from +3VLP



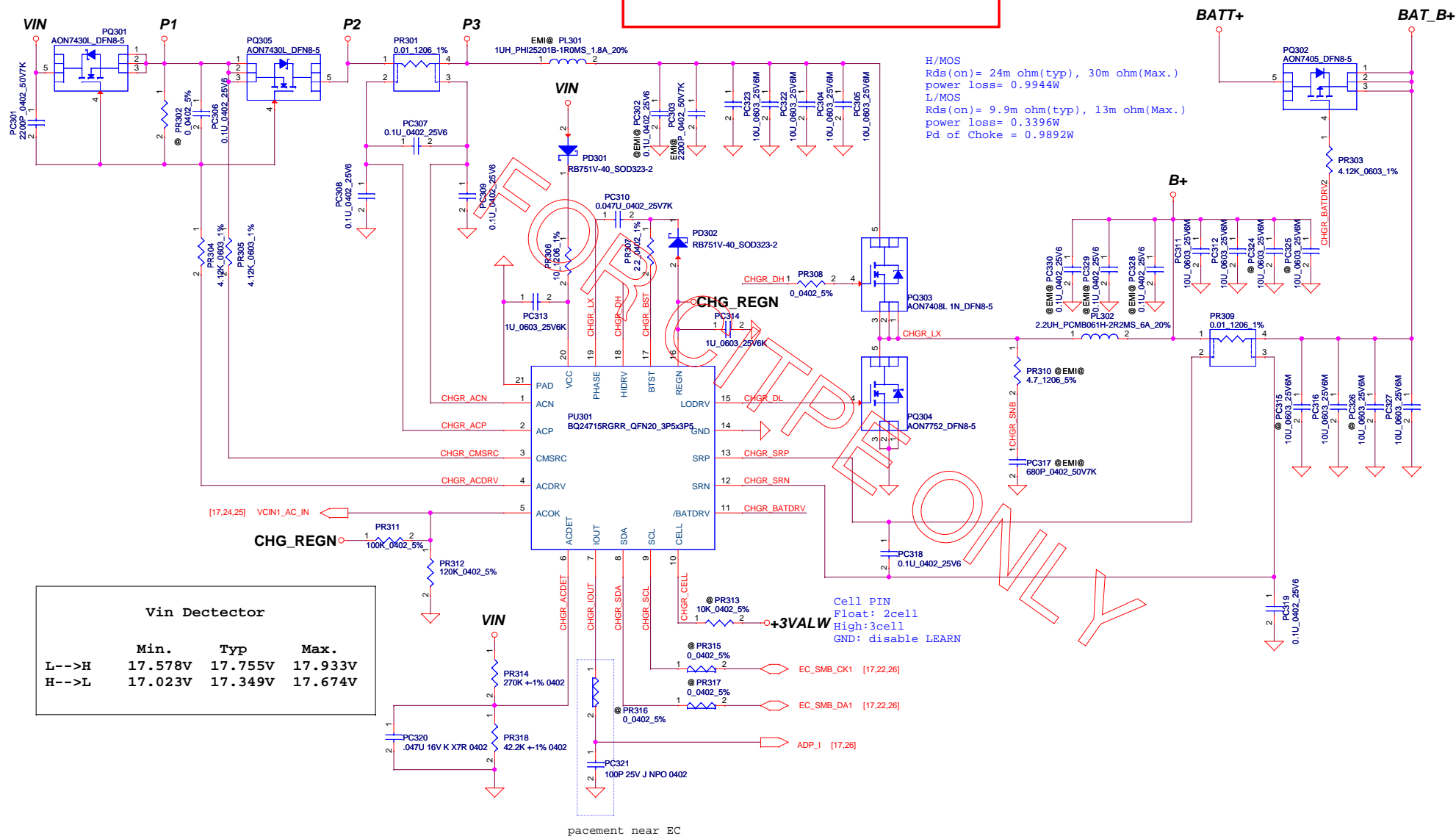
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				YOGA Paganini	1.0
				Date: Friday, October 17, 2014	Sheet 26 of 36

# Module model information

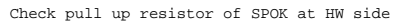
BQ24715\_V2.mdd

65W adapter support NVDC  
BQ24715 support 2, 3 cell  
BQ24717 for 4 cell



SYX196B\_V4.mdd

3.3V LDO 150mA~300mA



TDC=6A

TDC=6A

SYX196C\_V4.mdd

5V LDO 150mA~300mA

***Compal Electronics, Inc.***

**PWR-3VALW/5VALW**

**YOGA Paganini**

Rev  
1.0

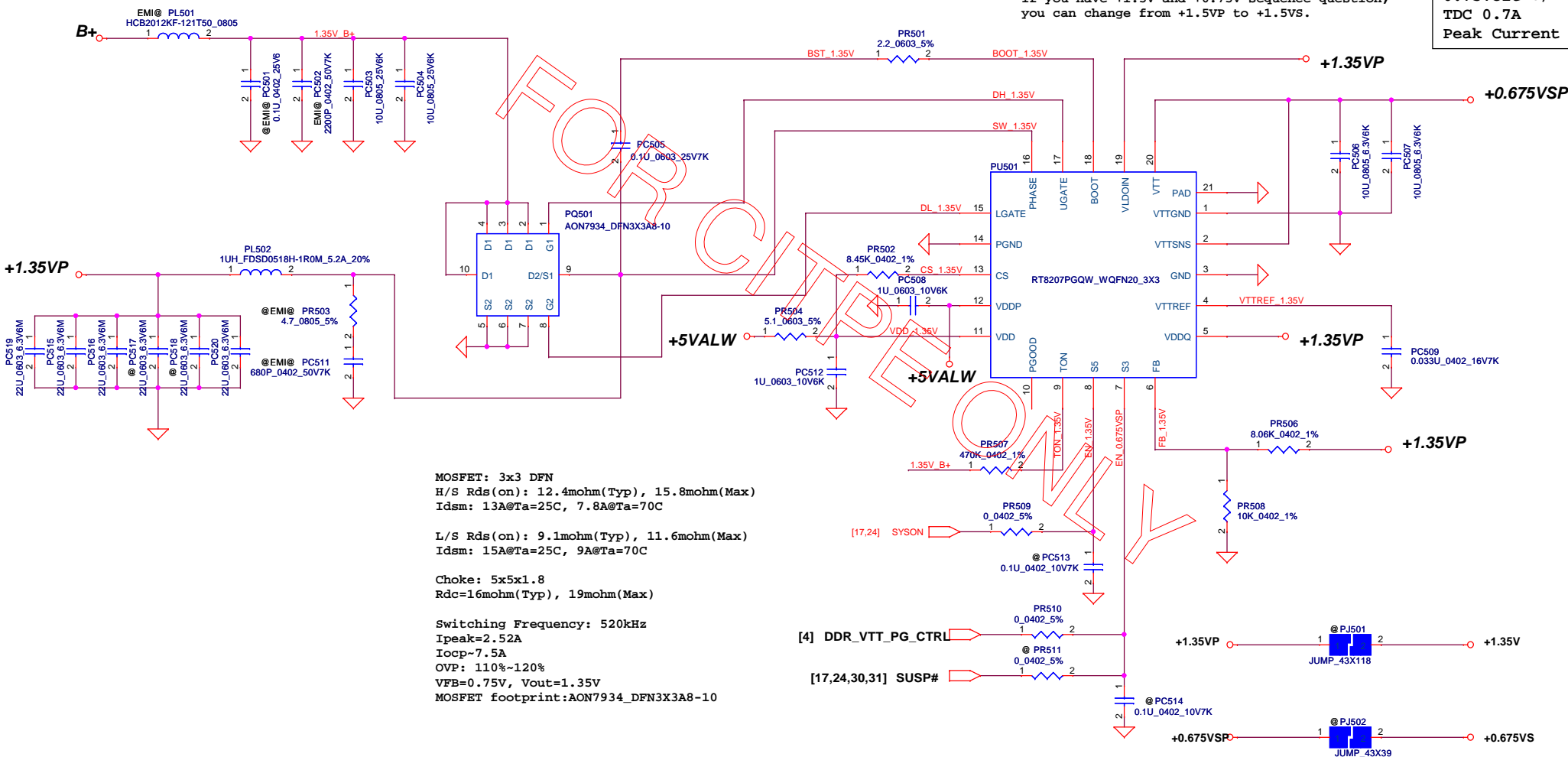
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# Module model information

RT8207M\_v1.mdd For Single layer  
RT8207M\_v2.mdd For Dual layer

Pin19 need pull separate from +1.5VP.  
If you have +1.5V and +0.75V sequence question,  
you can change from +1.5VP to +1.5VS.

0.75Volt +/- 5%  
TDC 0.7A  
Peak Current 1A

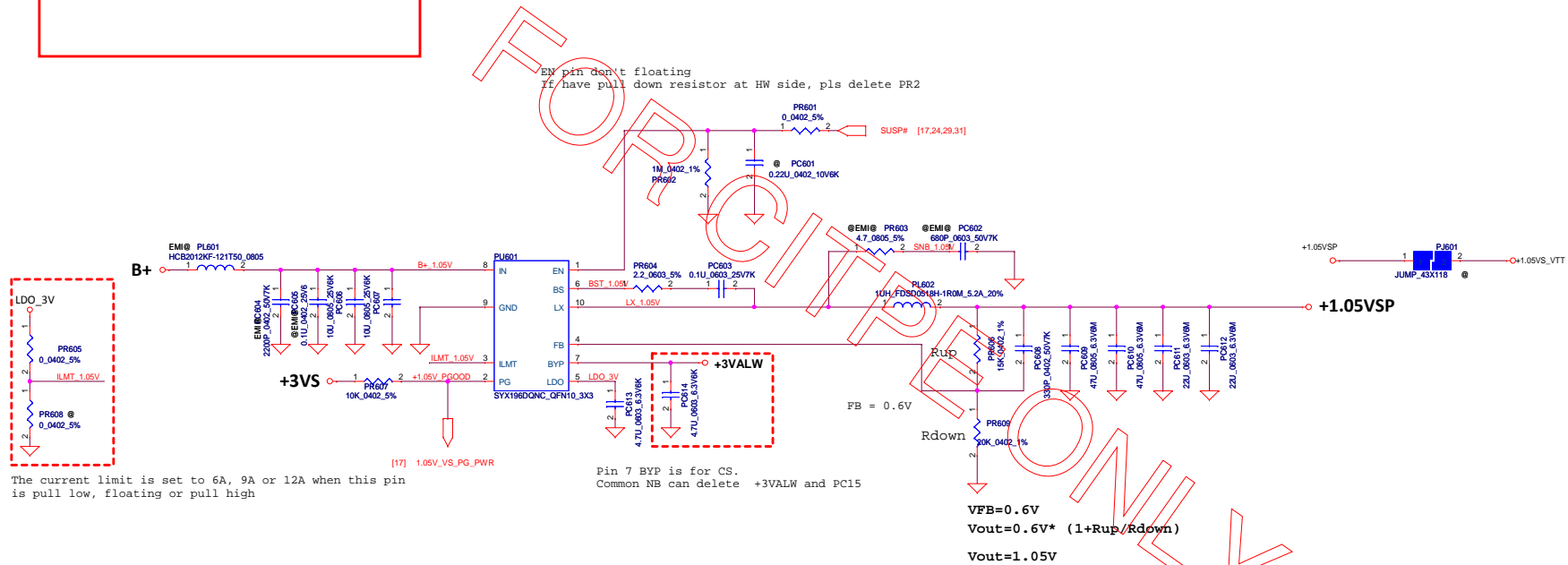


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Issued Date	2014/04/10	Deciphered Date	2017/04/10	Title	PWR-1.35V/0.675VS
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# Module model information

SYX196D\_V3.mdd

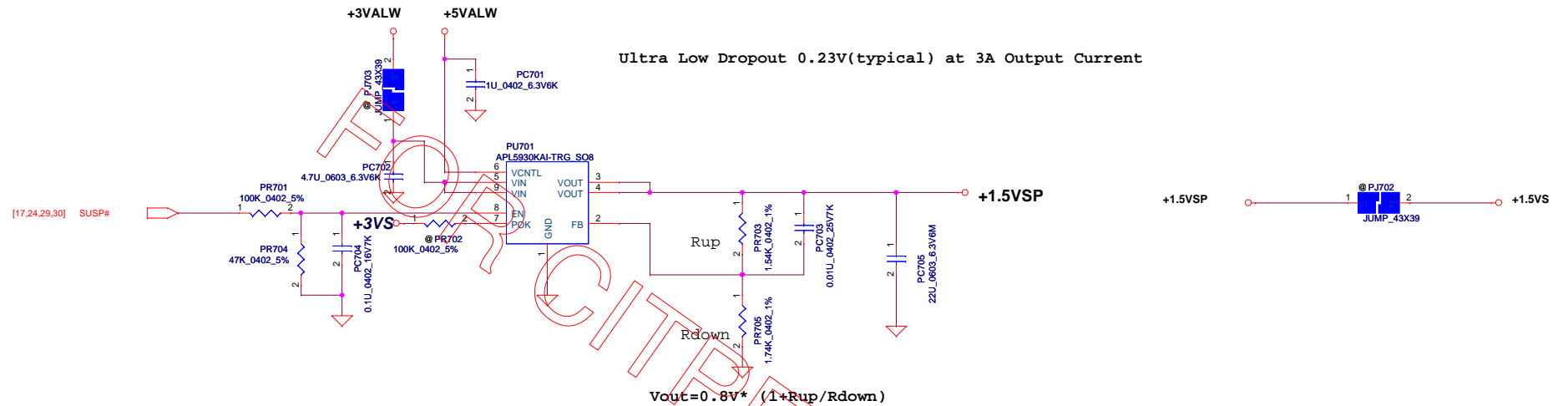
EN pin don't floating  
If have pull down resistor at HW side, pls delete PR2



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# Module model information

APL5930\_V2.mdd



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Module model information:  
ISL95813\_V1A for IC module  
ISL95813\_V1B for SW module

Base on BDW PDDG Rev\_1.2

Location	4.5W	
	TDC 8A	
	MAX 18A	
	OCF 27A	
	Loadline=-2.0mV/A	Note
PR820	1.27K Ohm	OCF
PR816	909 Ohm	Droop
PC816	0.047uF	RC Match
PR803	73.2kOhm	PROG1
PR806	102kOhm	IMON
PC817	@	RC Filter

Dual MOS: AON6932A  
Rds(on):  
@Vgs=10V  
Q1=4.1mohm  
Q2=1.7mohm  
@Vgs=4.5V  
Q1=6.7mohm  
Q2=2.4mohm

Choke: 0.22uH (Size:7\*7\*1.8)  
Rdc=4.3m ohm +5%  
Heat Rating Current=14A

+1.05VS\_VTT Follow intel guideline

Note:  
VR\_SVID\_ALRT# Pull high on HW side  
[10] VR\_SVID\_ALRT#

[10] VR\_SVID\_DAT

[10] VR\_SVID\_CLK

[10] VR\_ON

[10] VGATE

[17] IMON\_CPU

Note:  
VR\_HOT# Pull high on HW side  
[17] VR\_HOT#

Over temperature protection:  
OTP Setting: 100C active  
Pin5 (NTC) voltage <0.88V, Protect  
Pin5 (NTC) voltage >0.92V, recovery

Note:  
PR803=73.2K  
=>Icc(max)=18A  
fsw=700KHz

Note:  
PR512=124K  
=>Slew rate=53mV/us  
Vboot = 1.7V

Droop

RC Match

OCF Setting

Local sense put on HW site

CPU\_B+

B+

+CPU\_CORE

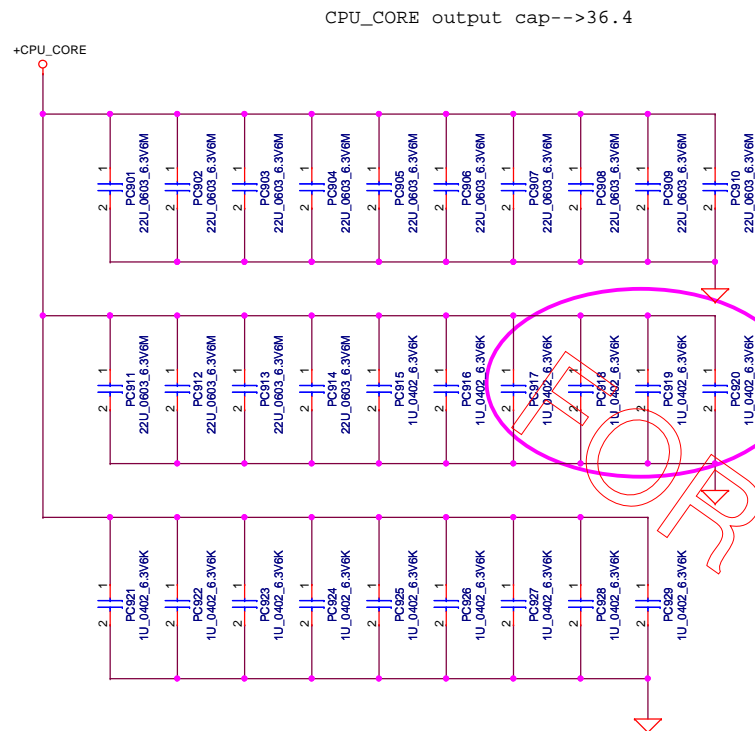


Compal Electronics, Inc.

PWR-CPU CORE

LA-B921PR10

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30 X 22uF 0805  
 2012/10/23  
 check the output cap Qty!!!  
 2012/10/24  
 23 pcs 22uF and reserve 7 pcs  
 2013/01/14  
 22uF\*15; reserve 22uF\*5

2013/09/6 22U\_0603x17 + 22U\_0805x2

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Item	Reason for change	PAGE	Modify List	Date	Phase
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				YOGA Paganini	
Date: Friday, October 17, 2014				Sheet 34 of 36	Rev 1.0

## Version change list (P.I.R. List)

Page 1 of 1  
for HW

Item	Reason for change	PG#	Modify List	Date	Phase	Verify
1	ME Request	P.20	H1,H2,H3 footprint change to H_3P3, Delete H6	2014-06-30	EVT-DVT	Pass
2	EMI request, for DCIN-USB port USB signal	P.22	Add L56(COM choke), R5223, R5224 to connect JDCIN1	2014-06-30	EVT-DVT	EA Pass
3	EMI request	P.15	CA32 replace to RA21, CA33 replace to RA24, CA34 replace to RA25	2014-06-30	EVT-DVT	Pass
4	EMI request	P.10	Reserve RC152 connect to JC1	2014-06-30	EVT-DVT	Pass
5	For fine tune I2C interface driving	P.8	RC130-RC133 change value to 2.2K ohm	2014-06-30	EVT-DVT	EA Pass
6	For ME Z-height limitation	P.19	C5274,C5275 replace to C5264	2014-06-30	EVT-DVT	EA Pass
7	For ME Z-height limitation	P.22	C5276,C5277 replace to C5267, C5273 change to mount	2014-06-30	EVT-DVT	EA Pass
8	For S5 power saving	P.24	U2301.4 change power rail from VL to +5VALW	2014-06-30	EVT-DVT	Pass
9	Reserve path for verify sensor function	P.22	Add 0 ohm R5226 to connect JIO1.12 and U11.85	2014-07-01	EVT-DVT	Pass
10	Reserve path for verify sensor function	P.17	Add 0 ohm R5225 to connect U52.4 and U11.84	2014-07-01	EVT-DVT	Pass
11	Reserve path for verify BT function	P.19	Add PU R5227 to connect BT_DISABLE_R and +3VS	2014-07-01	EVT-DVT	Pass
12	Follow Intel design guide	layout	Voiding the GND plane underneath the SATA signals pad of JSSD1	2014-07-01	EVT-DVT	EA Pass
Item	Reason for change	PG#	Modify List	Date	Phase	Verify
1	Z-high impact for thermal plate	P.11	CC49(22U)(0603) change to 10U*2(CC49,CC100)(0402)	2014-08-13	DVT-PVT	Pass
2	Z-high impact for thermal plate	P.10	CC26, CC27, CC28, CC30 change to 0402 type	2014-08-13	DVT-PVT	Pass
3	Reserve for Intel request	P.13	ADD CD54, CD55, CD72, CD73 connect to +0.675VS	2014-08-13	DVT-PVT	
4	Reserve for Intel request	P.13 P.14	ADD CD56-CD71,CD74-CD87 connect to +1.35V	2014-08-13	DVT-PVT	
5	Reserve For EMI request	P.15	ADD CA35 connect to DMIC_CLK	2014-08-13	DVT-PVT	
6	solve plug in/out USB device auto shutdown issue	P.19 P.22	C5264 replace to C5274,C5275; C5267 replace to C5276,C5277	2014-08-13	DVT-PVT	Pass
7	For EMI/Audio request, solve audio noise issue	P.15	CA32, CA33, CA34 change to RA41, RA42, RA43	2014-08-13	DVT-PVT	Pass
8	ME request, for FFC 夾持力 issue	P.22	JSD1 connector change symbol 4pin to 6pin	2014-08-13	DVT-PVT	Pass
9	For DFB request	P.19	JWLAN1 change symbol	2014-08-13	DVT-PVT	Pass
10	Reserve For ESD request		Add C5274, CC101, CC102, CD88, PC328, PC329, PC330, PC428,PC429	2014-08-18	DVT-PVT	
11	For ME request	P.20	Fix hole H9 Change to H_4P0, Add H12	2014-08-18	DVT-PVT	
12	For ME request	layout	JEDP1 change location placement	2014-08-18	DVT-PVT	Pass
Item	Reason for change	PG#	Modify List	Date	Phase	Verify
1	ATE request reserve Test point to burn in MAC	P.17	Add T84,T85,T86	2014-09-25	PVT-SOVP	
2	For ME request	layout	JEDP1 change location placement(move down 2mm)	2014-09-25	PVT-SOVP	Verify on SOVP
3	Reserve DCIN USB power SW EC control path	P.22	Add R5228,R5229,R5230 to connect U2905, U11, PD103	2014-09-30	PVT-SOVP	
4	Reserve for ESD protect	P.25	Add DCIN_USB_EN connect to PD105	2014-09-30	PVT-SOVP	

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# Paganini Power Sequence

